Optimizing Reflowed Solder TIM (sTIMs) Processes for Emerging Heterogeneous Integrated Packages

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Abstract— Reflowed indium metal has for decades been the standard for solder thermal interface materials (solder TIMs or sTIMs) in most high-performance computing (HPC) TIM1 applications. The IEEE Heterogeneous Integration Thermal roadmap states that new thermal interface materials solutions must provide a path to the successful application of increased total-package die areas up to 100cm^2. While GPU architectures are relatively isothermal during usage, CPU hotspots in complex heterogeneously-integrated modules will need to be able to handle heat flux hotspots up to 1000W/cm^2 within the next two years. Indium and its alloys are used as reflowed solder thermal interface materials in both CPU and GPU "die to lid/heat spreader" (TIM1) applications. Their high bulk thermal conductivity and proven long-term reliability suit them well for extreme thermomechanical stresses.

Voiding is the most important failure mode and has been studied by x-ray. The effects of surface pretreatment, pressure during reflow, solder flux type/fluxless processing, and preform design parameters, such as alloy type, are also examined. The paper includes data on both vacuum and pressure (autoclave) reflow of sTIMs, which is becoming necessary to meet upcoming requirements for ultralow voiding in some instances.

The paper also considers the use of solder TIMs in the context of alternative TIM applications and technologies, such as thermal greases, pads, and phase change materials, as well as liquid metals.

Keywords- Thermal Interface Materials, TIM, indium, metal TIM, solder TIM, sTIM, heat transfer, thermal resistance

I. INTRODUCTION

Removal of heat from active semiconductor die has long been an important factor in determining the utility and lifetime of logic devices. Joule heating results from electric current passing through the materials and sequence of interfaces on the active (junction) surface of semiconductor chips. The concentrated heat load must be conducted through first the silicon die and then the components of the complete thermal solution, finally passing to the ambient environment. The rate of heat flow is driven by the temperature gradient from the junction to ambient.

As the junction surface temperature rises, thermal electrons are more likely to jump the band gap and introduce bit errors. Additionally, thermally activated diffusion, electromigration, and environmental reactions degrade the semiconductor. Finally, as transistors shrink, they become more sensitive to high temperatures because of increased non-fatal manufacturing defects [1].

Ideally, junction temperatures (Tj) for silicon logic devices are kept within the operating range from -40°C to +110°C). In order to maintain a longer standard refresh time (T_{ref})[2] and thus maintain sync with the logic die, DRAM devices (DDR4/5) are limited to junction temperatures less than 85°C. While GPU processor chip architecture, by the nature of its repetitive cell structure, maintains a relatively consistent temperature across the die surface, CPUs will increasingly have hotspots of greater heat flux, as has been noted in the IEEE Thermal Roadmap [3] [Fig. 1].

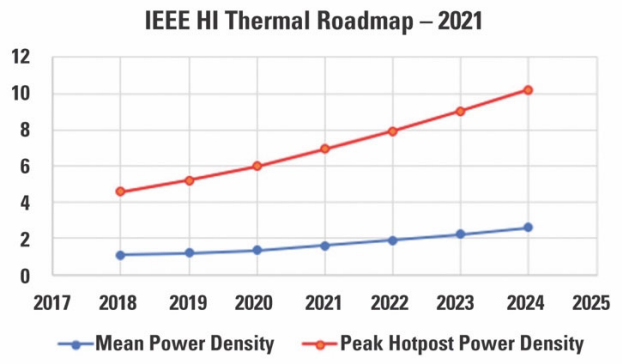

Fig. 1: Expectations of Heat Flux Intensity for Smallest Node by Year from IEEE Thermal Roadmap [3]

Devices manufactured at and below the 7nm node are no longer achieving the same energy efficiencies of scale as older nodes [4] and are therefore driving the increasing overall heat flux [Fig. 2].

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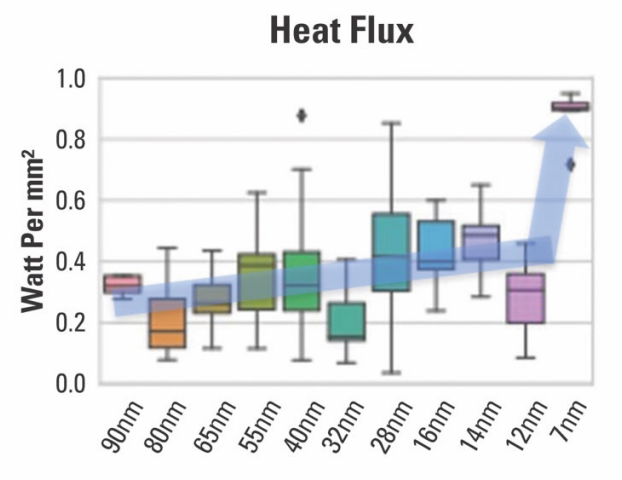

Fig 2: Mean Heat Flux by Wafer Fab Node [4]. Reproduced with lead author permission

The standard approaches to direct heat removal from logic and memory die are shown in Fig. 3. The methodology depends on a variety of factors, especially the required reliability and functionality of the silicon and package in the final system, as defined by its use case or mission profile.

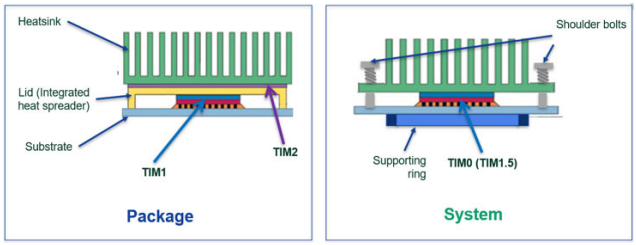

Figure 3: Types of TIM by Usage

A key factor is whether the packaged die should be treated as a separate component to be added into the system, or is actually an integral part of the system. More rugged applications such as automotive ADAS use the TIM1/2 package approach, while many AI modules use a pressurized TIM0 (TIM1.5) approach. Note that while the latter eliminates the need for reflow of the TIM during assembly, it also necessitates precision controls in manufacturing to minimize mechanical stress on the die during manufacture [5].

II. TIM Materials

A. Overview of TIM Materials

Thermal solutions are as varied as the devices they cool. In the simplest configuration, the back (top) surface of the die is coated with a conductive compound which, in turn, connects to the surface of a heat sink cooled by forced or natural convection. These compounds contain conductive particles to increase the thermal conductivity to several W/m-K. Recently, gallium-based liquid metal alloys (k ~30 W/m-K) have been used in some applications to provide high performance alternative solutions [6].

More complex thermal solutions include conductive lids permanently attached to the back of the die with a high conductivity interface (see Fig. 3: TIM1). This lid serves both as a protective cover, and as a heat spreader to distribute thermal loads laterally and orthogonally from the die surface. Composite epoxy and phase-change polymer TIMs have limited heat spreading capacity and are strongly affected by any assembly coplanarity issues.

In lidded packages, indium solder is the dominant thermal interface. Indium metal and its alloys used as sTIMs have proven their worth for many years for high-end logic devices. Indium metal provides a high thermal conductivity junction (k~86 W/m-K) between the die and lid. Unlike other solid metals, indium is compliant enough to conform to movement between the die and lid from differential thermal expansion strains. Indium anneals at room temperature, so it is not damaged by the cyclic plastic strain between the lid and the die. Indium-silver alloys (k~70 W/m-K) are similarly used in packages requiring additional reflow cycles.

As a contrast to compliant TIMs, gold alloys (for AuSn20, k~57 W/m-K) provide solutions where the bond and alloy are strong enough to deflect the package to absorb thermal strains. These gold alloys have a lower constant of thermal expansion (CTE) of 15 ppm/C compared with indium (32 ppm/C) so thermal mismatch strains are smaller. However, the high tensile strength of AuSn20, not to mention its cost, limits its use to smaller die only.

The high conductivity of metal is due to the majority contribution of electronic phonons rather than lattice vibrations. Polymers have limited thermal carrying capability since the conductive pathways are via low frequency vibrations of C-C bonds. These phonon modes are at the opposite end of the spectrum from thermally conductive ceramic powders that are used to increase bulk conductivity. This frequency/phonon mismatch between the fluids and fillers creates a thermal pathway with multiple interfacial resistances. In the case of metallic TIMs, however, the electronic phonons universally couple between the metal TIM and the interface surfaces, with only oxides and intermetallics potentially increasing the junction thermal resistances.

In all cases, a sTIM has the inherent metal attribute of isotropic conductivity. The conduction cone of a point source therefore expands as heat passes through the metallic TIM. This behavior spreads the heat from a concentrated source. This is especially important as the die are thinned and the concentrated junction heat sources are coupled with the first level TIM.

B. Solder TIMs

To reap the benefit of the high conductivity and reliability of the sTIM, the solder and the soldering process must produce high reliability solder joints. Both the heat spreader and the back side of the die must have an adherent, solderable surface. The component reliability depends on the life of both these transition interfaces and of the solder.

The sTIM indium preforms are made to exacting requirements. The raw materials, as well as the casting,

fabrication and packaging of preforms are all tightly controlled, and the manufacturing process is automated. The TIM assembly process is also controlled and automated. Note that the beneficial properties of indium can be lost if the parts are mishandled—the softness of indium makes the surfaces very susceptible to dents, scratches and collecting foreign materials. Any of these incidents can result in voids in the finished sTIM.

A benchmark paper by Intel [7] first openly discussed the use of indium metal as a thermal interface material. The metallizations of the back side of the die and lid provide the soldering surfaces to reliably join silicon to copper with indium. On both sides of the joint, indium is anchored to nickel with a protective gold finish. Nickel forms a stable intermetallic bond with indium. The solubility of nickel in the indium is very low so diffusion-controlled growth of the intermetallic (IMC) layer is slow. On exposure to air, nickel forms a unsolderable oxide on its surface, so it is protected with a flash coating of gold. In reference [7], an optimum gold thickness was determined. At the low end, the gaps in the plating resulted in voiding. At the high end, excess IMC growth occurred during reflow and reliability testing.

The bondline thickness (BLT) of indium solder preforms is typically at least 100 µm (4mils). This thickness is determined by the difference in thermal stresses between the die and the lid. The layer of indium must absorb most of the strain to minimize stresses on the die. The area of the sTIM preforms is typically slightly smaller than that of the die, and the preforms must be precisely placed to eliminate edge voids and solder extrusion. A standard 30-50um BLT collapse must also be allowed for when designing the lid coining depth (inside height of lid) to prevent solder extrusion.

III. Lidded Processors

A. Assembling Lidded Processors

The overall process flow for solder TIM1 is shown in Fig. 4 below and detailed later in the paper.

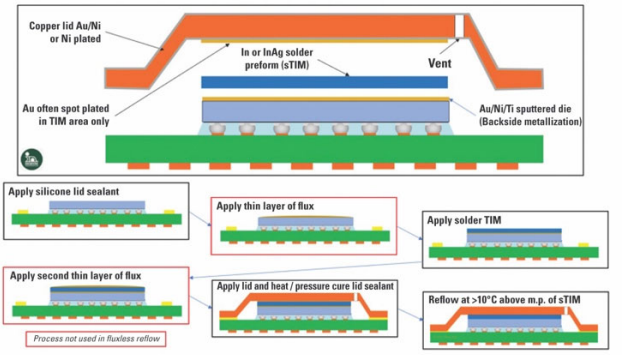

Fig. 4: Process Flow for a Typical sTIM with a Vented Lid

B. Failure Modes

When the substrate deflects away from the lid during thermal cycling, or any reflow (assembly / precon) processes, non-wet failures can result (Fig. 5). After assembly, joint quality is inspected using x-ray or confocal scanning acoustic microscopy (CSAM). CSAM provides a depth-adjustable image of the interfaces—showing voids, delamination and other interfacial defects. In fig. 5, the solder preform has melted and balled up before wetting: the negative ("smiley") substrate deflection amounted to about 50% of the 150µm BLT.

Fig. 5: CSAM of sTIM Failure Due to Substrate Negative Deflection

An upward bow in the substrate will force the sTIM out from the bondline, creating extrusion failures. A properly designed sTIM1 assembly produces an interface with full coverage and no overflow (Fig. 6). Any small coverage deficiencies or overflows can be corrected with adjustments of the assembly preload. The post-reflow solder BLT collapse can be adjusted by changing either the coining depth of the lid or adhesive thickness.

A liquid "flux" material, if used, (see Fig. 4) prevents movement of the preform when the lid is applied. A second application of flux to the preform follows its placement. The lid seal is applied to hold the lid in place, and the assembly is fixtured lid seal cure. The curing step fixes the degree of compression on the solder TIM.

Fig. 6: CSAM of Good sTIM after Reflow

In the reflow oven, the flux is activated (reacts with metal oxides to form salts) during preheating (below 150°C). This preheat removes the flux solvent and facilitates the reaction of metal oxides and activators in the flux. The solder step melts the solder and forms the interfaces with the die and the lid. The hold time and peak temperatures are optimized for the heating equipment (box or line furnace) and the thermal mass of the assembly. The heating profile is a balance between longer and hotter for initial interface quality, and shorter and cooler for minimizing IMC growth. The cooling rate through solidification relaxes residual stresses.

Die fabricated at smaller nodes can generate higher heat flux hot spots. Voiding is therefore not desirable from a local

thermal resistance point of view. Voiding in the thermal interface material is typically characterized by the x-y (in same plane as the TIM) area as a percent of the overall TIM coverage area. There is an increasing trend amongst solder TIM users towards both defining both a lower overall voiding (%max void total), and a maximum allowable void size or areal percentage, with the technology drivers already discussed for advanced nodes.

IV. IMPORTANCE OF SURFACES

Oxides and surface contamination prevent good wetting of molten solder onto solderable surfaces [8] and hence are associated with voids. The metal surfaces to be joined using sTIM are usually gold, with the silicon backside typically being PVD-deposited Ti/NiV/Au (80-200nm Au), and copper heatspreader/lids plated with Ni/Au (usually with 0.3-0.8um Au). Except for the inevitable presence of a film of adventitious carbon [9] and nickel oxidation due to pinholes in the gold, the surface of gold will not change with time.

The thickness of indium oxide (In_2O_3) follows a parabolic growth curve [10]. As a solid the growth rate is minimal. A sample in air at 145°C (m.p. of indium is 157°C) shows the oxide layer growing to 2 nm in 5 minutes. This increases to 4 nm after 2 hours, and this number is used as an upper bound of oxidation during storage.

V. OXIDE REMOVAL AND FLUXING

In sTIM reflow, indium oxide (In_2O_3) is removed by reaction with mild liquid organic fluxes (e.g. Indium Corporation's 5RMA) or formic acid/N_2. The use of formic acid as a reducing agent for tin (Sn) based reflow soldering has been widely studied and globally applied. Gas phase formic acid in an inert gas (usually N_2) can be injected during the reflow process, removing the metal oxide and promoting proper wetting and solder reflow. Generally speaking, the reaction is [11]:

$$HCOOH + SnO \rightarrow Sn(COOH)_2 + H_2O$$

An oxygen-free atmosphere prevents reoxidation of the metal. The exact mechanism for elimination of the formate is still under debate, and one leading theory is sublimation at elevated temperatures [12].

In addition, when heated to above 180°C, formic acid undergoes thermal decomposition [13]. There are two potential pathways:

Dehydration

$$HCOOH \rightarrow CO + H_2O$$

Decarboxylation:

$$HCOOH \rightarrow CO_2 + H_2$$

The CO and H_2 byproducts from this thermal decomposition might contribute to the metal oxide reduction but given the slow reaction at typical lead-free reflow temperatures (<260°C), they are not likely to be dominant.

The reaction for indium oxide is suspected to be similar to that of tin oxide. The resultant indium formate is eliminated through sublimation.

$$HCOOH + In_2O_3 \rightarrow In(COOH)_3 + H_2O$$

VI. CAUSES OF VOIDING

Several types of solder voids have been noted [14], most of which are related to the solder metallurgy. The type of void considered in the current study is referred to as a "macro void", occurring mostly within the bulk solder itself.

Voiding (strictly "macro voiding") is best described as the formation of fluid cavities in solder during reflow resulting in bubble-like inclusions in the final reflowed solder joint. Voids are metastable, in that the combination of forces present - both on the surface of the void (energy from the surface tension measured in N/m or J/m^2), and compressive and buoyancy forces on the void - should cause the bubble to burst, drastically reducing the overall potential energy. It should therefore be obvious that there is a factor acting as a potential energy barrier, essentially pinning the void in place. The key factors preventing the bubble bursting are:

- Poor wetting on adjacent solderable surfaces, trapping the void against the surface
- Dishing (concavity) of upper surface
- Trapping by rough surface intermetallics, or by the solid content of a solder below its liquidus (within the "pasty range")
- Oxide or other contamination on liquid metal surfaces creating a steric hinderance

This last factor has been shown to be a major consideration allowing stable but oddly shaped bubbles in aqueous liquids stabilized by small particles [15]. Molten solders and liquid metals can be expected to behave similarly.

Studies on solder voiding are multifarious, using a variety of different solder types and applications, but are mostly focused on mechanical reliability [16], rather than their thermal aspects.

The impact of voids of various sizes and locations on theoretical thermal resistance (Rth) of sTIM, from spherical to cylindrical voids has been evaluated in depth [17] using both analytical and numerical methods. Lack of capability to manufacture voids appropriately prevented experimental verification. An almost linear dependence of overall thermal resistance as a function of void volume fraction was noted for small (0.04mm) voids, while larger voids (0.12mm) showed a power law dependence. They also noted that the spatial distribution of voids has a major impact on Rth.

VII. EFFECT OF PRESSURE ON VOIDS

Minimizing the size of voids in solder can be done by two means:

- Creating an external low pressure or vacuum to grow the void to the point where it bursts [18]
- Increasing the pressure on the void to shrink it

The Laplace equation governing internal pressure (Pi) of a bubble submersed in a liquid is:

$$Pi = (2\gamma / r) + Po$$

Where γ is the surface tension, r is the radius and Po is the outside pressure. Using realistic values for solder surface tension, the impact of pressure on bubble size can be seen (Fig. 7).

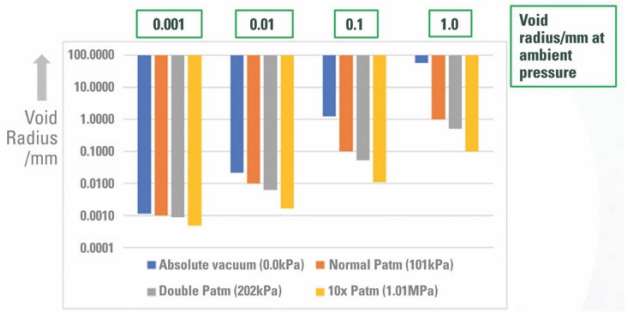

Fig. 7: Theoretical Relationship Between External Pressure and Void Size

The effect of varying external pressure on smaller bubbles is therefore minimal, while larger bubbles are easy to expand and allow to burst by creating an external vacuum, or shrink by increasing the external pressure.

VIII. HELLER AND INDIUM CORPORATION STUDIES: KEY VARIABLES

Two experimental setups were designed to accomplish differing tasks – one used at Indium Corporation and the other at Heller Industries.

For Indium Corporation, the task at hand is to establish a low-cost test vehicle capable of detecting even subtle variations in voiding performance for both current indium metal, $InAg_x$ and future materials development. This requires increased sample sizes and bulk processing. This study also investigates the effect of subsequent higher temperature reflow (mimicking SAC solder ball attach for BGA) on TIMs voiding. Fig. 8 below shows an x-ray result after sTIM reflow, then after subsequent SAC reflow (details later).

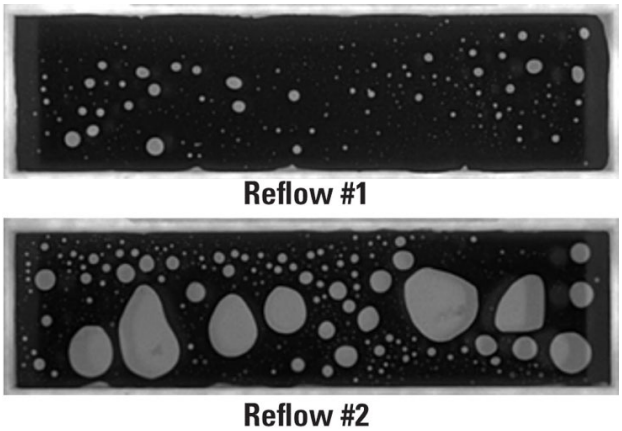

Fig. 8: Reflow#1 vs. Reflow#2 – same part

In the case of Heller Industries, the task was to establish the various equipment and processing/profile effects on voiding using baseline 99.99In solder preforms. The impact of these changes is far larger and allows for individual test subjects closer resembling real world die packages to determine future pathways from the equipment side.

A. Indium Corporation: Experimental

In this experimental design, the key input (independent) variables are the solder alloy, reflow profile and number of reflows while the measured (dependent) variable is overall void percent. The key control variables are the test setup and prebake conditions which were held constant for the purposes of this study. The goal of this initial work is to investigate the impact of each input variable on the voiding behavior of the test subject. Primarily, the differences in alloy composition and their effect on the voiding % during initial and subsequent reflows were explored. This will serve as the foundation for future work on other key variables such as varying reflow profiles (time/temperature/atmosphere), preform thickness, flux %, test vehicle, metallization and surface cleanliness – among potential others. The initial DOE is summarized in Table 1.

Table 1: Description of input and control variables in initial DOE

Alloy (%)	Preform Dimensions	Preform Thickness	Flux	Flux (wt.%)	Reflow Profile #1 (Low-Temp Reflow)	Reflow Profile #2 (Low-Temp Reflow)
99.99In	1.26" x 0.35"	0.009"	LV2K	0.5	Peak Temp.: 165°C TAL: 110s Atmosphere: N_2	Peak Temp.: 255°C TAL: 110s Atmosphere: Air
97In/3Ag						
90In/10Ag						

B. Test Method and Materials

All samples were processed using an identical test setup (Fig. 9).

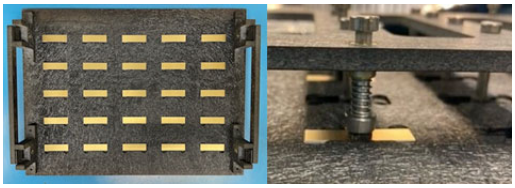

Fig. 9: [Left] 25 specimens before lid is placed. [Right]Side view once lid is placed – the springs can be swapped out to change the force applied

The pragmatic purpose of this design is to roughly simulate a die/solder TIM/heatsink package in a way that is highly cost efficient and generates statistically valid data (25 data points).

The general process flow is shown in fig. 10. The test subjects themselves are individual stacks, or sandwiches, consisting of an ENIG-plated FR4 substrate on either side with solder preform between. The solder alloys used were either 99.99In, 97In/3Ag, and 90In/10Ag. Importantly, they were pre-flux coated during the manufacturing process with

LV2K (ROL0 per J-STD-004B) flux coating and produced to match the substrate size with a 1:1 ratio. All solder and flux TIM products used are commercially available.

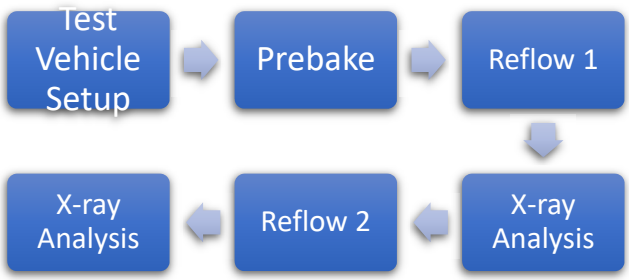

Figure 10: Basic flow chart of the experimental procedure.

For the prebake step, the entire test setup is placed inside a static oven at 135°C for 1 hour. Each individual stack is under a pressure of 5-6 psi (35-41kPa) during this process. After cooling, the test vehicle is run through a convection reflow oven using the desired reflow profile. At this stage, a solder joint has been formed and voiding analysis is completed using a DAGE Quadra 7 X-Ray Inspection System. The entire test vehicle is then sent through the reflow oven again and subsequently re-analyzed for voiding. Using this process, the voiding behavior from an initial low temperature reflow and successive high temperature reflow(s) can be distinguished.

C. Results

Fig. 11 summarizes the voiding results between the three different metal compositions, ranging from pure indium (99.99% purity) to InAg10 while Table 2 shows the corresponding quantitative trend data.

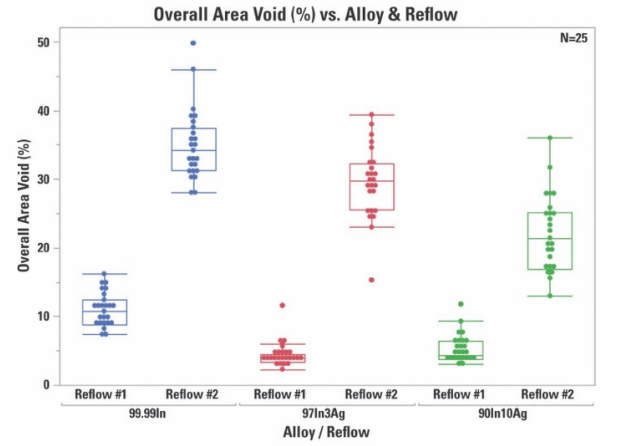

Figure 11: Solder TIM composition vs void % separated between reflow #1 and reflow #2

Table 2: Summary Derived from Data in Figure 11

Alloy	Reflow #	# of Samples	Mean Void %	Lower 95%	Upper 95%
99.99In	1	25	10.76	9.18	12.35
99.99In	2	25	34.91	33.33	36.50
97In/3Ag	1	25	4.24	2.65	5.83
97In/3Ag	2	25	29.48	27.90	31.07
90In/10Ag	1	25	5.26	3.67	6.85
90In/10Ag	2	25	22.06	20.48	23.65

A Tukey-Kramer means comparison carried out using JMP® statistical software confirms that there is a statistically significant difference between all samples except 97In/3Ag Reflow #1 and 90In/10Ag Reflow #1. This is also reflected by these being the only sample conditions with overlapping confidence intervals in Table 2 ($\alpha = 0.05$). Additionally,91% of all variation comes from the combination of alloy and reflow conditions as opposed to random variation within test conditions. Based on these factors, we can conclude that the differences between test conditions (alloy and reflow #) are real and represent true differences. Flux wt% (0.25% vs 0.50%) was also screened but showed no significant difference in void %.

D. Discussion

Increasing the silver (Ag) content in indium preforms from zero to 10% (by weight) gives reduced voiding during initial reflow. It is interesting to note that good solderability to the gold surface is achieved, even though the liquidus temperature of InAg10 is much higher than the peak temperatures reached in these experiments.

E. Heller Industries: Experimental

The work carried out at Heller Industries was focused primarily on the effects of a standard older style of TIM flux, 5RMA (where a separate flux was used), and the effects of various pressures and atmospheres: formic acid reflow, vacuum reflow and high pressure reflow. Vacuum and formic processes can be accomplished sequentially using the same temperature / pressure / atmosphere profile, in a single horizontal reflow oven. For this reason, many of the test legs were completed utilizing both methods.

F. Vacuum and Formic Acid Reflow Testing

A formic reflow process does not use an organic flux. Formic acid vapor is injected into the process environment at the oven's soak zones, and reacts as described previously with metal oxide [19,20].

Organic flux residues trapped within solder can outgas and create voids [21], and this is minimized when using a fluxless process with formic acid. For this study, formic acid concentration was a key variable that was explored: concentrations were measured at zone 5, and were held between 2-5% for the relevant tests.

Vacuum reflow utilizes a vacuum chamber placed after the peak zone in a reflow oven. Samples enter the chamber while the solder is above its liquidus, and this peak temperature is maintained inside the chamber via infra-red (IR) heaters. Once the sample is inside the chamber, the chamber is sealed and evacuated to a controlled low pressure: bubbles within the liquid solder expand and burst leaving the solder almost void-free.

The key control variables related to vacuum reflow explored in this study are pressure (vacuum level), and dwell time under reduced pressure. Tests involving vacuum in this study used pressure levels between 20 – 150 Torr (2.7 to 20kPa) and dwell times of either 20 or 40 seconds.

All vacuum and formic tests were performed on a Heller 2043 Vacuum Formic Reflow (VFAR) oven, consisting of 10 convection heating zones, a vacuum chamber with 5 IR heating zones, a formic vapor injection system, and a mesh belt conveyor. Continual N2 flow kept oxygen levels in the process environment between 40-50 ppm throughout the reflow process.

The thermal profile used for the vacuum and formic tests is shown below in Fig 12. The profile has a soak time between 130-150°C of 151 seconds, a peak temperature of 189°C, and a total time above 180°C of 596 seconds. An earlier profile was tested which had significantly shorter times above liquidus. These runs provided poor void rates and are not included in the results. Formic concentrations were also measured in all zones with a binary gas analyzer to map the formic profile. The formic profile used for the 4-5% peak formic runs are shown in table 3.

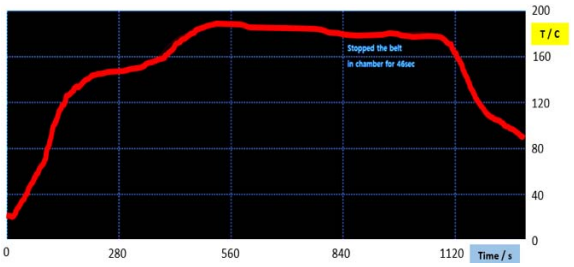

Fig. 12: Thermal profile used for vacuum and formic testing.

Table 3: Formic concentration profile used for 4-5% peak formic test legs.

	Zone 1	Zone 2	Zone 3	Zone 4	Zone 5	Zone 6	Zone 7	Zone 8	Zone 9	Zone 10
0_2 PPM	60	50	50	40	40	40	40	50	40	40
Formic Range	2–3%	3–4%	3–4%	3–4%	4–5%	4–5%	4–5%	4–5%	4–5%	3–4%

G. High Pressure Reflow Tests

A high pressure reflow oven is an autoclave. The sample is heated above its liquidus and pressurized with nitrogen gas. Pressure is maintained as the solder cools and solidifies, resulting in shrinking of voids. High pressure reflow does not use formic acid so an organic flux was required, and was applied beneath and on top of the sTIM (Fig 4). Key variables investigated for the high pressure reflow study were the pressure profile, thermal profile, and amount of flux applied to the preform.

All high pressure tests were performed on a Heller Pressure Reflow Oven (PRO). An image of the pressure oven with a diagram of the chamber heating is shown in Fig 13. The temperature profile used for the high pressure tests is shown in Fig. 14. The PRO is enabled with a vacuum pump which could be utilized to purge the chamber for purposes of removing volatiles formed from the applied flux. Each test performed on the PRO utilized two separate vacuum purges for this purpose. Each purge would drop the pressure inside the chamber to -1 Bar, and held for 20 seconds. After the second vacuum purge, pressure was increased to either 5 Bar or 10 Bar for the duration of the reflow cycle.

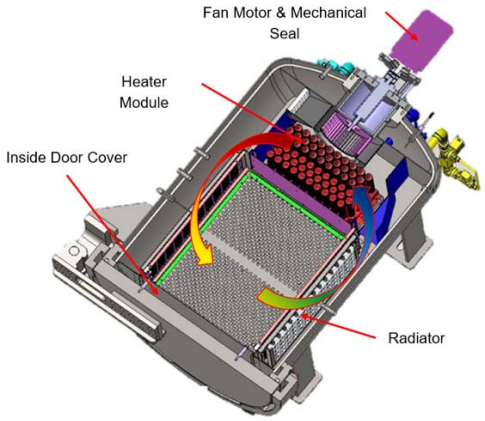

Figure 13: Pressure Reflow Oven (PRO) Chamber

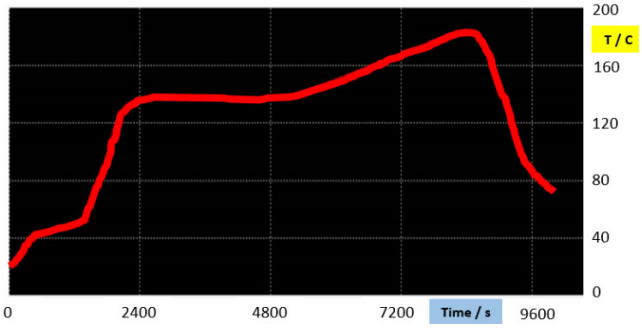

Figure 14: Thermal profile used for high pressure reflow tests

H. Test Vehicles and Test Vehicle Design

Test vehicles used were created by mounting a sputtered Silicon die to standard FR4 using a room temperature epoxy. A solder preform and lid were then placed on top of the die, and a graphite fixture was utilized to keep the components properly positioned and held the in place. This helped to ensure an even bond line was formed. Flux was also added to both sides of the preform for samples used with the high pressure reflow tests. During testing, no external pressure was applied to the top of the lid. A diagram of the assembly is shown in Fig 15 and a photograph in Fig. 16.

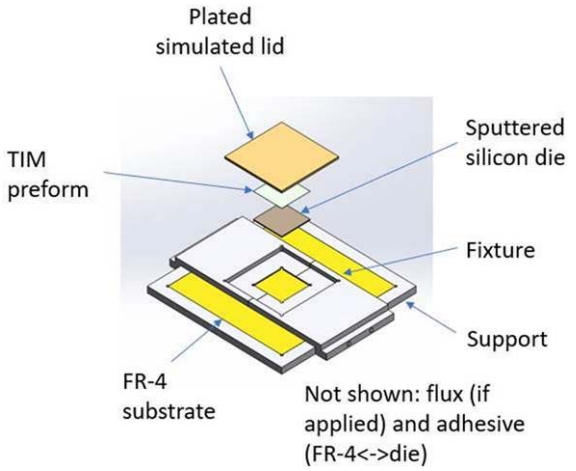

Fig 15: Test vehicle assembly containing lid, preform, die, FR4 and graphite fixture

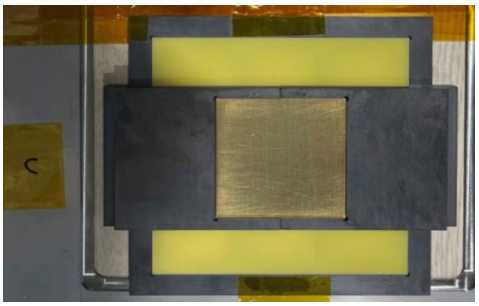

Fig 16: Actual Test Vehicle Assembly

Three different plated "lid" metallizations were studied: Au 0.5µm + Ni 0.5µm, Au 0.25µm + Ni 0.5µm and Ni 0.5µm. For the bulk of the investigation only the Au 0.5µm lid type die were used. Again, in these latter experiments, vehicle cost prohibited multiple repeats, but the differences from both visual inspection of the x-ray results and the calculated total voiding data are demonstrable.

I. Results

The results are summarized in the below tables (4 and 5). Fig. 17 to 23 show x-ray photographs of the actual specimens from which the total voiding is derived.

Table 4: Vacuum and Formic Acid Results

Leg	Lid Type	Peak Formic Concentration	Vacuum (Torr)	Dwell (s)	Void Rate
34	Au0.5µm	2–3%	No Vacuum		1.6%
35	Au0.5µm	4–5%	No Vacuum		2.2%
36	Au0.5µm	4–5%	100–150	20	1.1%
37	Au0.5µm	4–5%	20	20	2.3%

Table 5: High Pressure Reflow Results

Leg	Lid Type	Flux Above and Below Preform	Void Rate
32	Au0.5µm	5mg + 5mg	9.8%
33	Au0.5µm	15mg + 15mg	13.2%

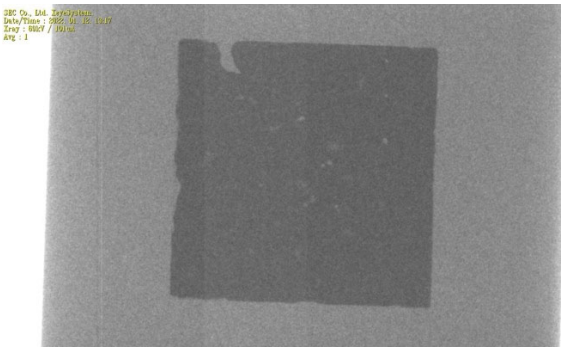

Fig 17: Formic: Leg 34 – Void Rate 1.6%

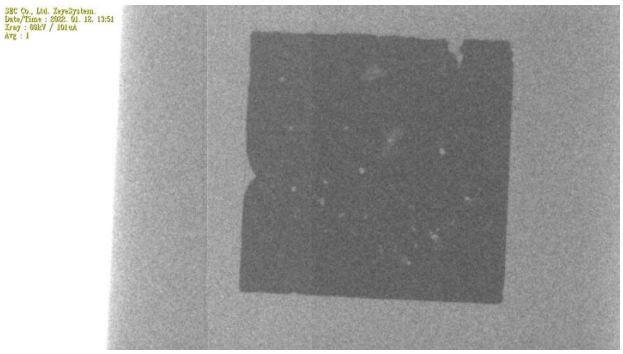

Fig: 18: Formic: Leg 35 – Void Rate 2.2%

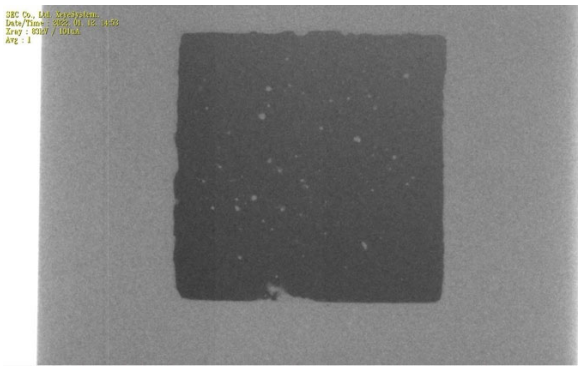

Fig. 19: Formic: Leg 36 – Void Rate 1.1%

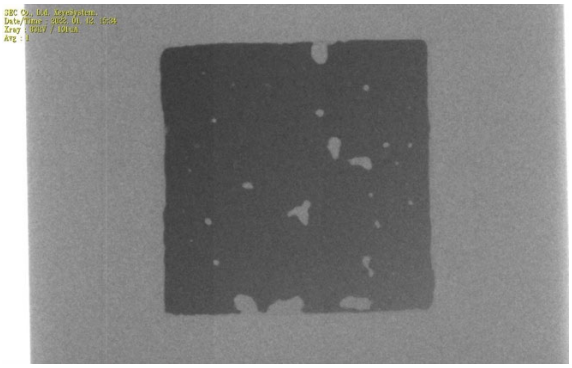

Fig. 20: Formic: Leg 37 – Void Rate 2.3%

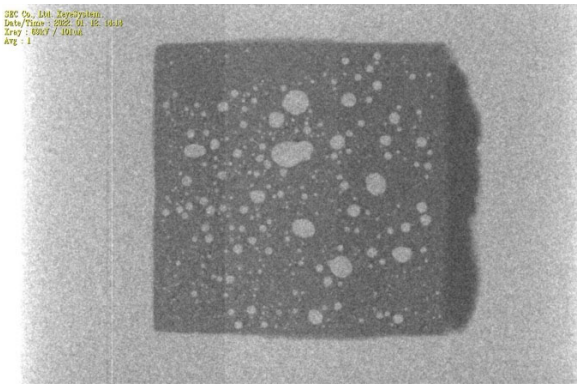

Fig. 21: Leg 32 – Void Rate 9.8%

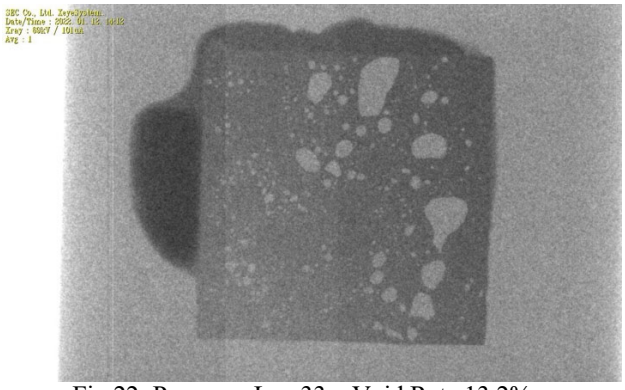

Fig 22: Pressure: Leg 33 – Void Rate 13.2%

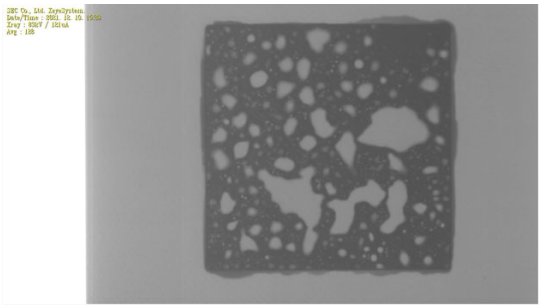

Fig. 23: Pressure: *Non-optimized High Pressure Reflow Result - Void Rate 36.4%*

This investigation into how various process parameters effect the void rates for TIM1 lid attach has led to several key findings:

- Lowest voiding was seen using formic acid reflow rather than organic flux
- Any impact that vacuum reflow has on void rates with formic acid is marginal
- The optimal time above liquidus is significantly longer than with typical soldering
- Pressurized reflow with flux yields better results than atmospheric reflow with flux, however it is not as good as atmospheric reflow with formic acid
- Pressurized reflow leads to extrusion (solder outflow from the die edges) (fig. 21, 22)

IX. FUTURE WORK

In the next year, further work will focus on:

- The impact of multiple subsequent reflows and profiles (including lower peak temperatures) on void rates
- Improving fixturing to give more consistent wetting near die edges
- Optimizing the time above liquidus (TAL) for the atmospheric formic tests to determine if TAL can be shortened without increasing void rates
- Power cycling: Utilize active die to determine actual heat flux through the Indium TIM1 and lid at 100-150W/cm^2
- Effect of plasma cleaning of lid and die backside (initial studies show no effect on lids)
- Flux formulation optimization, using halogen-free, ultralow residue and VOC-free types, as flux is often used as tackifier as well as a reducing agent
- CSAM and 3D x-ray to determine void location in x, y and z dimensions, and get further to root cause

X. CONCLUSIONS

The increasing usage of heterogeneous integration will lead to increasing complexities in manufacturing assemblies and stresses during system lifetime (Fig. 24): from more benign but long service-life AI server environments to the harshness of ADAS EV and military/aerospace ambient environments and stresses.

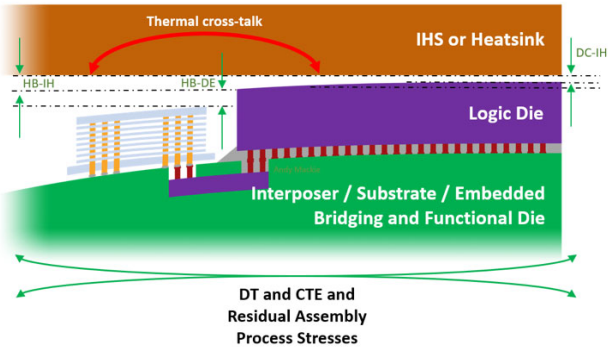

Fig. 24: Stresses in HI modules

This increase in complexity also means that the integration of thermal interface materials into high-level systems, especially TIM1 and TIM0, is occurring not just at subcons and OSATs, but increasingly as a post-BEOL process in high-end wafer fabs. This places a much greater emphasis on supplier ability to meet "semi-quality" expectations.

Metal-based TIMs in the form of structurally-reinforced materials; more compressible materials; liquid metals and liquid-metal based pastes and novel composites are either already available or near commercial release.

Materials and equipment vendors alike are aligning to bring complete thermal solutions to our mutual customers, as we have demonstrated in the current work.

XI. Acknowledgements

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XII. References

[1] Sperling, Semiconductor Engineering https://semiengineering.com/predicting-reliability-at-3-2nm-and-beyond/
[2] Cho et al. "Innovative Indicator to Evaluate DRAM Cell Transistor Leakage Current Distribution", Journal of the Electron Devices Society, pp. 494-499, Volume 6, 2018
[3] IEEE Heterogeneous Integration Roadmap found at https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html
[4] Sun et al., "Summarizing CPU and GPU Design Trends with Product Data", arXiv:1911.11313v2 [cs.DC] 13 Jul 2020
[5] Greenlaw, "Making KGD silicon work in your supply chain", Keynote speech at Known Good Die workshop, 2020
[6] Mackie et al. "Evolution of thermal interface materials for advanced packaging", Chip Scale Review, pp.55-60, May-Jun 2021
[7] Deppisch et al., "Material Optimization and Reliability Characterization of an Indium-Solder TIM for CPU Packaging" pp 67-74, JOM, June 2006
[8] Conseil et al., "Contamination profile of Printed Circuit Board Assemblies in relation to soldering types and conformal coating", Proc. EuroCorr 2014
[9] Piao and McIntyre, "Adventitious carbon growth on aluminium and gold–aluminium alloy surfaces", Surface and Interface Analysis, 33(7), 591, July 2002
[10] Kim et al., Journal of Electronic Materials, pp. 483-489, 37(4), 2008
[11] Lin, Wei, and Y. C. Lee. "Study of fluxless soldering using formic acid vapor." IEEE transactions on Advanced Packaging 22.4 (1999): 592-601
[12] Mokhtari, Omid, et al. "Characterization of tin-oxides and tin-formate crystals obtained from SnAgCu solder alloy under formic acid vapor." New Journal of Chemistry 43.26 (2019): 10227-10231.
[13] Martin, Schmeiber. "Decomposition of formic acid." Physics. chem-ph (2011).
[14] Aspandiar, "Voids in Solder Joints", SMTA Boise Expo and Tech Forum, March 20, 2018 inter alia
[15] Subramanian et al., "Non-spherical bubbles", Colloid Science, NATURE, Vol 438(15), December 2005
[16] Yunus et al., "Effect of voids on the reliability of BGA/CSP solder joints", 26th IEEE/CPMT IEMTS, San Diego, 2000
[17] Okereke and Ling, "A computational investigation of the effect of three-dimensional void morphology on the thermal resistance of solder thermal interface", Applied Thermal Engineering 142 (2018) pp. 346–360
[18] Yeo et al., "Vacuum Reflow Process Characterization for Voidless Soldering Process in Semiconductor Package", 38th IEEE IEMT Conference, 2018
[19] Ross et al., "Low voiding solder joints for multiple reflow applications", US patent 9468136
[20] Ross et al., "Low voiding solder joints for multiple reflow applications", US patent 9010616
[21] Diehm et al., "Reduction of Voids in Solder Joints and Alternative to Vacuum Soldering", IPC APEX EXPO, 2012